## REMARKS

### *Summary of Amendments/Status of Claims*

Claim 1 has been amended to incorporate the limitations of claim 17 and to address the § 112 rejections of this claim. Claim 1 thus limits the bottom face and perimetric wall entirely constituting the recess in the ceramic substrate's wafer-retaining face both to forming an angle of from 90° to 170°, and to joining in a curvature of at least 0.1 mm.

Dependent claims 9-15, independent claim 17 itself and its dependent claims 18-20 thus having been rendered redundant over amended claim 1 and its dependent claims 2-8, claims 9 through 20 have been canceled.

Claims 1-8 thus are pending reconsideration on the merits.

### *Claim Rejections – 35 U.S.C. § 112*

Claims 1-20 were rejected under 35 U.S.C. § 112, first and second paragraphs, in particular for the phrase, added to both independent claims 1 and 17 by Applicant's RCE-accompanying amendment dated January 14, 2008,

> the bottom face being sized to receive a back side of the wafer such that the back side is in contact with the bottom face across substantially the entire diameter of the wafer.

The Office regards the above-quoted phrase as failing to comply both with the written-description as well as the definiteness requirements of the statute.

These rejections have been addressed by amending claim 1 in such a way that the recitation allegedly failing to comply with requirements of § 112 is now fully supported by the specification as filed. That is, the phrase "across substantially the entire diameter of the wafer" has been stricken from claim 1. Meanwhile, it is respectfully pointed out that paragraph [0018] of the specification as filed states

> [A]s far as the form of the wafer pocket is concerned, it . . . may have a flat bottom face of size to allow for accommodatingly carrying a wafer,

while immediately ensuing paragraph [0019] states,

> For example, as illustrated in Fig. 1, a wafer pocket 5 consisting of a recess having a depth that is about the same as the thickness extent of a wafer 6 is provided in a ceramic susceptor 1. Placing the wafer 6 onto the flat bottom face 5a of the wafer pocket 5 accommodates the wafer 6 within the wafer pocket 5.

The specification thus clearly states that the recess bottom-face is flat; at the same time, Fig. 1 clearly shows—in a fragmentary, shorthand manner—the back side of a wafer 6 (in phantom) flush with the recess bottom face 5a. Since wafers for

semiconductor-device fabrication are by definition flat, it follows that a person skilled in the art would understand the present inventors to have had possession of the claimed feature that "the bottom face [is] sized to receive a back side of the wafer such that the back side is in contact with the bottom face."

At the same time, it is respectfully submitted that inasmuch as the phrase "substantially the entire diameter" has been stricken from claim 1, the rejection of the claims as being indefinite on account of this phrase has been overcome.

***Claim Rejections – 35 U.S.C. § 103***

Claims 1, 2, 5, 6, 9, 10, 13, 14, 17 and 18: *Sato et al.*

Claims 1, 2, 5, 6, 9, 10, 13, 14, 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Sato et al.* (Japanese Unexamined Pat. App. Pub. No. 2002-134484, machine translation).

The rejections made in the July 12, 2007 Office action, made final, on the merits have essentially been upheld, and in fact to begin with in the current action have been repeated by their incorporation by reference.

Claims 9-20 have been canceled; below Applicant addresses the rejection of claims 1, 2, 5 and 6 over *Sato et al.*, and in so doing refers to the July 12, 2007 Office action, inasmuch as the reasons of record for the rejections have been incorporated by reference into the present action, as just noted.

As the Examiner states in the Office-action letter of July 12, 2007, the Sato et al. publication does not specifically show either that the angle that the bottom face and the side make is 90 to 170°, nor that the curvature R of their boundary portion is 0.1 mm or more, but would have it that as a general matter, optimizing the angle and the curvature is obvious.

Nevertheless, in Figs. 3 and 5 of *Sato et al.*, the bottom section *itself* has a slant or curvature, which is clearly distinct from amended claim 1 of the present application. And although in Fig. 4 of *Sato et al.* a recessed section with a flat bottom face appears, it is clearly smaller than the wafer diameter; thus because the flat bottom face (as opposed to the inclined sides) of the *Sato et al.* bottom section is not of a size that can accommodate the wafer, *Sato et al.* likewise differs from amended claim 1 of the present application. These distinctions should now be particularly clear from claim 1 as amended, which now recites,

> a recess formed in said wafer-retaining face with room to carry a semiconductor manufacturing wafer, said recess constituted by a perimetric wall and a bottom face the entirety of which is planar, . . .the bottom face being sized to receive a back side of the wafer such that the entire back side is in contact with the bottom face.

In contrast to claim 1 of *Sato et al.*, which has it that "the semiconductor substrate is retained with only the circumferential margin of its rear side contacting the inclined surface of the recessed section," the present invention, as given in paragraph [0017] of the present specification, is constituted so that the entire wafer insets into the wafer pocket:

> As a result of investigating means for suppressing heat radiation from the circumferential surface of a wafer, the present inventors took note of the ways in which wafers are set onto ceramic susceptors for semiconductor manufacturing equipment, and came up with providing a recess that can accommodatingly carry a wafer (. . . also referred to as a "wafer pocket") in the face of the ceramic susceptor on its wafer-retaining side.
>
> Here, as far as the form of the wafer pocket is concerned, it may be sunken to an extent lower than the ceramic-susceptor face on its wafer-retaining side, and may have a flat bottom face of size to allow for accommodatingly carrying a wafer.

Accordingly, with *Sato et al.* the external diameter of the bottom face is smaller than the wafer, but with the present invention as claimed, the external diameter of the bottom face is larger than the wafer; this difference is clearly distinct.

In addition, with *Sato et al.* all that is discussed is to control, as separate embodiments, the angle of the substrate holder's bottom-face section and the curvature of its bottom-face section, (*Sato et al.* Fig. 3 is ultimately bottom-face section angles, while Fig. 5 is ultimately bottom-face section curvature); nothing whatsoever is stated regarding the angle that the bottom-face section and the peripheral section form, nor regarding the boundary portion between the bottom-face and peripheral sections.

Moreover, no instance or example is disclosed of adapting the angle and curvature at the same time. In particular, no mention is made anywhere regarding how curvature of the boundary between the bottom and the peripheral sections ties in with cracking.

Furthermore, with *Sato et al.*, the discussion is of optimizing bottom-face angle or bottom-face curvature so that an interval from the wafer will be produced, but as set forth in the present specification at the end of paragraph [0018]—which was quoted from above—and the beginning of paragraph [0019],

> [T]he wafer pocket preferably is a circular depression whose outer diameter is approximately the same as that of the wafer, but is not thereby limited.
>
> For example, as illustrated in Fig. 1, a wafer pocket 5 consisting of a recess having a depth that is about the same as the thickness extent of a wafer 6 is provided in a ceramic susceptor 1.

Thus, any interval between the wafer and the bottom section is significantly small, as is clear from the drawings in the present specification.

To begin with, then, the case with *Sato et al*. is, as in claim 1 thereof, that a large gap is deliberately produced between the wafer and the wafer-carrying face, to make the wafer contact along a line, but the case with the present invention as recited in claim 1 is to accommodate the entire wafer, and make it so that any space between the wafer and the wafer-carrying face is kept approximately the same. Thus being of completely the opposite concepts, there is an enormous disparity in the manner of thinking between *Sato et al*. and that of the present invention as claimed.

While in a manner of speaking, *Sato et al*. presents the main impeding factor to the claimed content of the present application, nevertheless, for the foregoing reasons, it is respectfully submitted that the rejection of claims 1, 2, 5 and 6 over *Sato et al*. in light of the knowledge of, or even what might be routine experimentation by, a person skilled in the art has been overcome.

Claims 3, 4, 7, 8, 11, 12, 15, 16, 19 and 20: *Sato et al*. in view of *Soma et al*.

Claims 3, 4, 7, 8, 11, 12, 15, 16, 19 and 20 were rejected as being unpatentable over *Sato et al*. as applied in making the rejection addressed above, in view of U.S. Pat. No. 5,231,690 to *Soma et al*.

Claims 9-20 have been canceled. Applicant points out in the first place that with regard to *Soma et al*., the form of the wafer-carrying face is uninterruptedly flat, such that it differs completely from the structure recited in claim 1 of the present application, in which a wafer is retained in a recessed section.

Moreover, Applicant addresses the present rejections by further pointing out that with *Soma et al*., it is evident that the structure is not furnished with the plasma electrodes recited in claims 5-8 of the present application.

And Applicant also notes that while *Soma et al*. recites the material for the resistive heating element being W, Mo and Pt, only these three metals are mentioned, whereas in the present application, other than these three metals, Pd, Ag, Ni and Cr are also disclosed.

Finally, Applicant notes that with regard to the material for the ceramic susceptor, while *Soma et al*. sets forth the two substances $Si_3N_4$ and AlN, in the present application, other than these two substances, $Al_2O_3$ and SiC are also disclosed.

Above all, since the claims rejected over *Sato et al*. in view of *Soma et al*. each depend either directly or indirectly from claim 1 and thus carry with them all of the limitations of claim 1 and any intervening claims, and since claim 1 is, for the reasons argued above in addressing the § 103 rejection of claim 1 over *Sato et al*., believed to be allowable, it is respectfully submitted that claims 3, 4, 7 and 8 should also be held allowable.

Claims 1-20: *Hirotake et al.* in view of *Soma et al.*

Claims 1-20 were rejected as being unpatentable over *Hirotake et al.* (Japanese Unexamined Pat. App. Pub. No. 2000-290773, machine translation) in view of *Soma et al.*

Claims 9-20 have been canceled; below Applicant addresses the rejection of claims 1-8 over *Hirotake et al.*, and in so doing again refers to the July 12, 2007 Office action.

With regard to *Hirotake et al.*, the Office-action letter of July 12, 2007 in paragraph 14 discusses a "wafer-retaining face," but as far as *Hirotake et al.* is concerned, the reference relates not to a ceramic susceptor that carries wafers, but to a method of manufacturing bulk ceramic materials that are deposited by CVD; nothing whatsoever is mentioned about the carrying or loading-on of wafers.

*Hirotake et al.*, is a reference in which merely a way of manufacturing material by CVD is disclosed—in which the technical field totally differs from that of the present invention.

Further, in *Hirotake et al.*, while there is discussion concerning cracking in the deposited bulk ceramics, there is absolutely no discussion with regard to the cracking in ceramic susceptors (substrates) that is discussed in the present application.

Still further, neither in the deposited ceramic nor in the deposition substrate of *Hirotake et al.* is a heater incorporated.

Therefore, *Hirotake et al.* differs completely from the "recess . . . with room to carry a semiconductor manufacturing wafer, said recess including . . . a substantially planar bottom face" recited in claim 1 of the present application, nor does the reference meet the susceptor heating element recited in the present application.

It is respectfully submitted that claim 1 as amended thus distinguishes over the *Hirotake et al.* even in combination with *Soma et al.*, and that it follows that the remainder of the pending claims rejected over *Hirotake et al.* in view of *Soma et al.*, being properly dependent on claim 1, distinguish over *Hirotake et al.* in view of *Soma et al.* and should therefore be held allowable.

***Conclusion***

From the foregoing arguments, it is respectfully submitted that the technical fields of *Sato et al.* and *Hirotake et al.* are different from that of the present invention, and thus it would be extremely difficult for a person skilled in the art to combine them.

Ultimately, *Sato et al.* is an attempt to define the bottom-face angle/curvature for situating a wafer so that it is out of contact with the bottom section; *Sato et al.* does

not define the present invention's angle between the bottom face and the periphery (perimetric wall), nor the curvature R of its boundary-line portion.

Furthermore, with *Hirotake et al.*, as also argued above, there is altogether no relation to ceramic susceptors that carry wafers; moreover, although Fig. 1b sets forth a curvature, the cited example given is one in which the peripheral portion in its entirety has the curvature R, which is a matter that utterly runs counter to the boundary line between the bottom face and the peripheral portion having a curvature R, as stipulated by claim 1 of the present application.

Taken together, neither *Sato et al.*, *Hirotake et al.*, nor, for that matter, even *Soma et al.* discloses a given example of the boundary line between the bottom face and the peripheral portion being a curvature R.

Accordingly, there is no cited reference that *prima facie* shows at the same time both the angle formed by the bottom face and the peripheral portion, and the curvature R of their boundary portion. Moreover, it is respectfully submitted that, given the context of the references as analyzed above, the Office has not presented a proper rationale whereby a person skilled in the art would find it predictable to combine the references.

As fully supported in paragraphs [0018] and [0019] of the present specification to begin with, the present invention as set forth in claim 1 reduces thermal radiation from the circumferential surface of a wafer placed on the claimed susceptor, to enable enhanced temperature uniformity in the heated wafer. Meanwhile, lending the boundary portion of the bottom and peripheral sections of the recess a curvature of at least 0.1 mm makes it possible to prevent cracking in the ceramic susceptor.

Accordingly, Applicant courteously urges that this application is in condition for allowance. Reconsideration and withdrawal of the rejections is requested. Favorable action by the Examiner at an early date is solicited.

Respectfully submitted,

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